holistic energy harvesting

PRiME www.prime-project.org

Run smarter
Live longer!

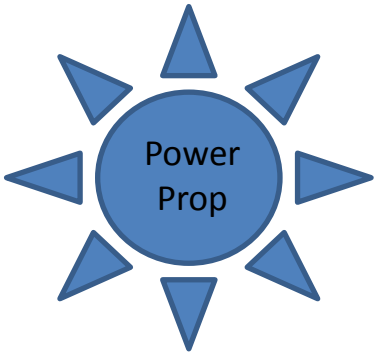
Newcastle University

Putting Microsystems Design on a Strict diet

Alex Yakovlev
microSystems
EEE School

Energy Theme
Lunchtime Talk
26 January 2015

efuturesXD

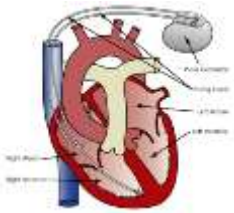


The more you get
The more you give!

Agenda

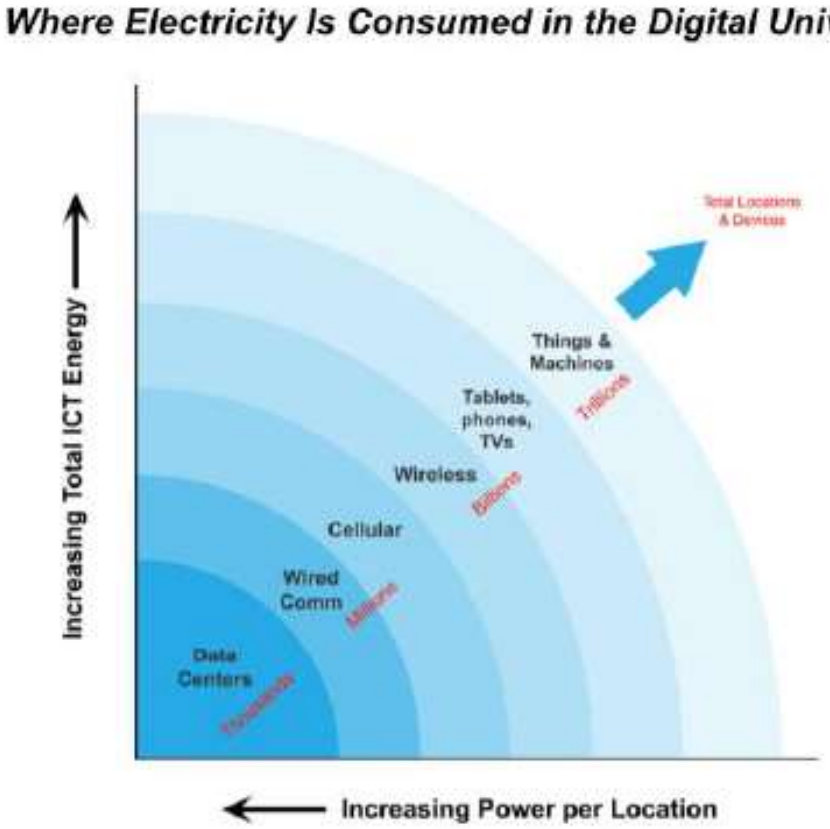
- **Why do we explore energy/power issues in uSys?**
- **Energy Theme in our Research Layers**
  - **Basic: concepts, principles, theories, models**
  - **Applied: themes, design methods, tools, systems, exploitation routes**
- **Research projects:**
  - **Recent and ongoing (Holistic, SAVVIE, PowerProp, PRiME, A4A)**
  - **Key academic and industrial collaborations**
  - **Future plans**
- **Key Challenges**

Why do we explore energy/power issues in uSystems?



“Propaganda”

- The energy consumption by the world ICT ecosystem amounts to 1,500 TWh per year, which is about 10% of the world electricity generation (or combined total of Germany and Japan) [M.P. Mills report 2013, “Cloud begins with Coal”, http://www.tech-pundit.com/]



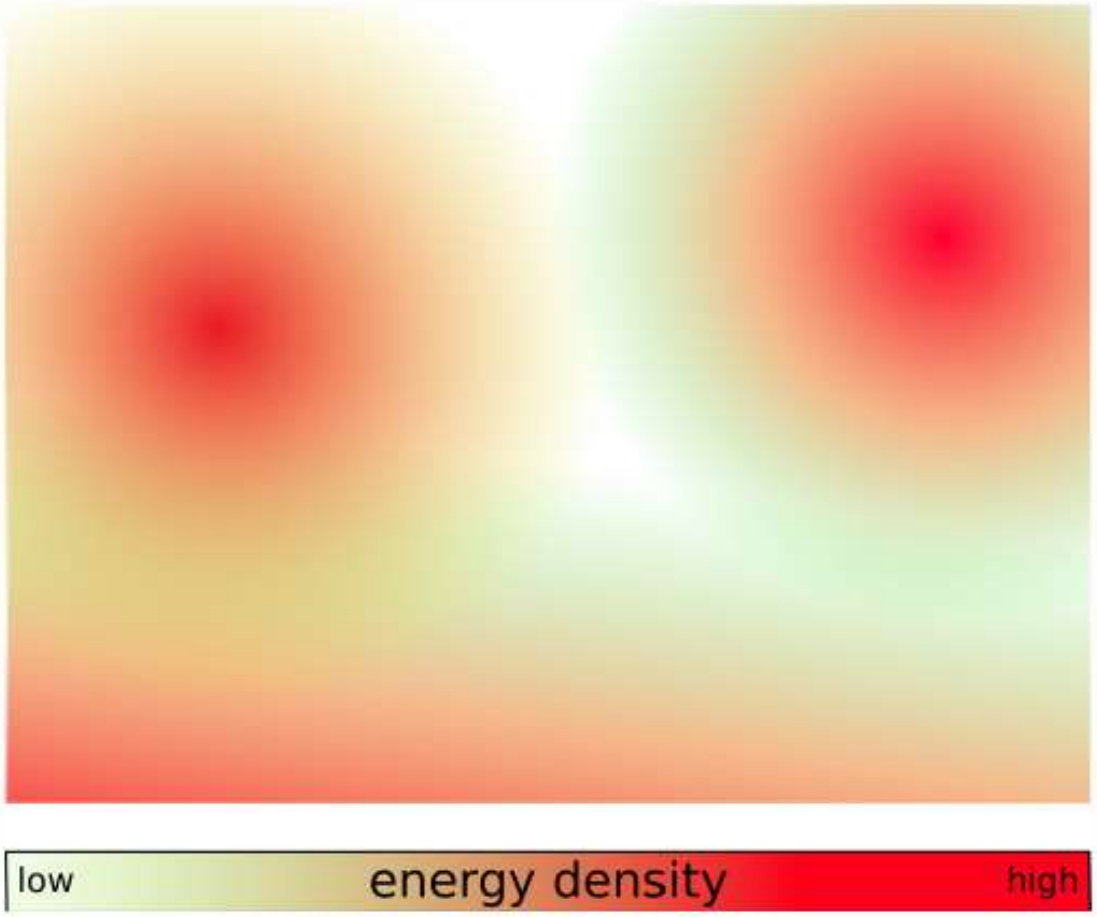
- Issues: Battery life, electricity bills, power inaccessibility, overheating, noise’s …
- A wealth of events, papers, etc. in the ICT domain bears adjectives: energy-efficient, energy-aware, energy-conscious, green, energy-saving, …

Motivation comes from:

- **Electronics Technology Evolution**
  - Approaching end of the road on device scaling in CMOS
  - Unsustainable growth in power consumption
- **Society and Applications**
  - Energy generation, conservation, utilisation
  - Health, Aging, Well-being
  - Environment, Climate
  - Transport, Urban
  - “Specific EEE/CS App Trends”: implantable devices, wearable devices, IoT, Cloud, Big Data, Smart Grid …
- **Bringing Energy & Information together has always been an intriguing intellectual challenge!**

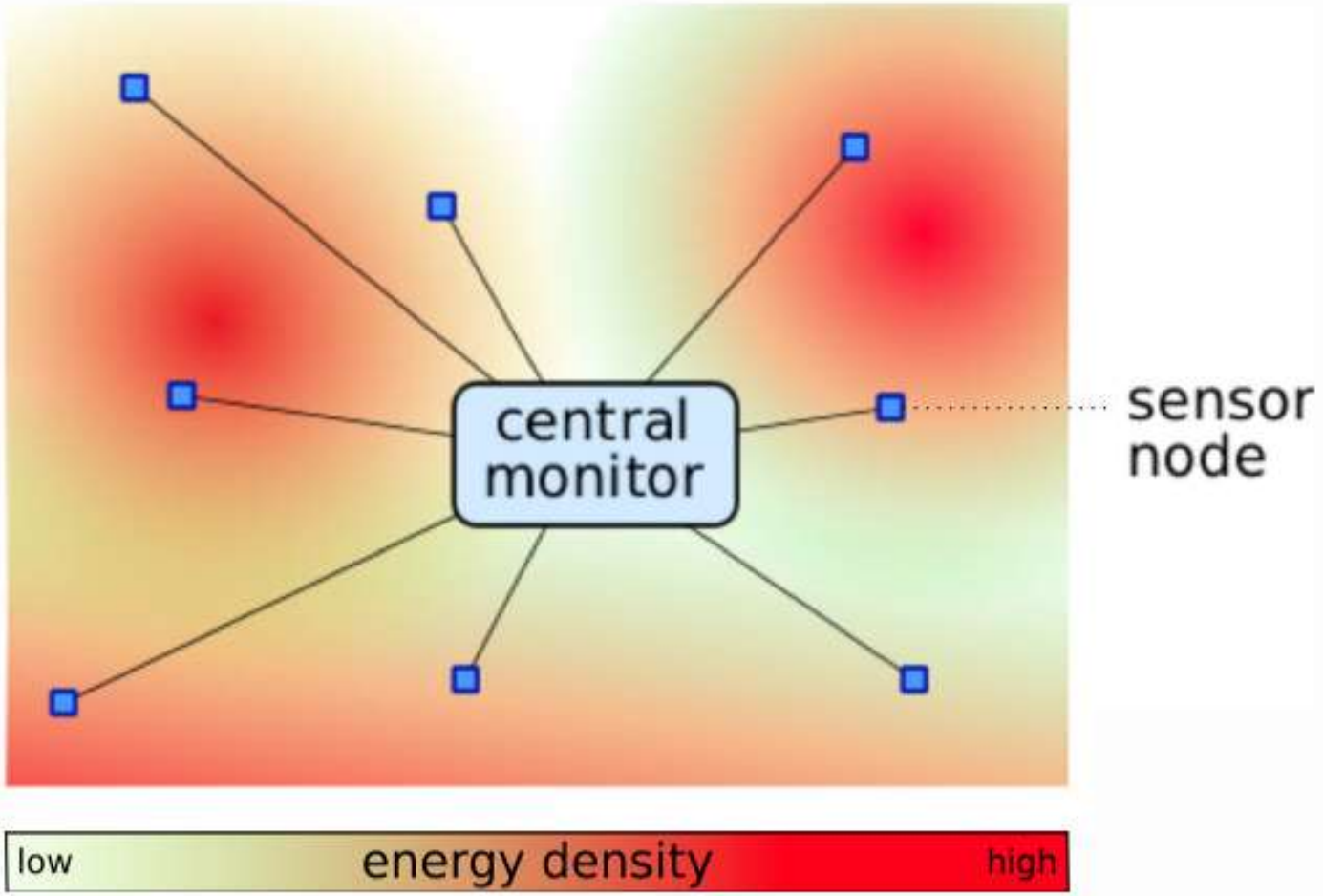
Example: Walls Alive (condition monitoring)

- Energy field (thermal, mechanical vibration, etc)



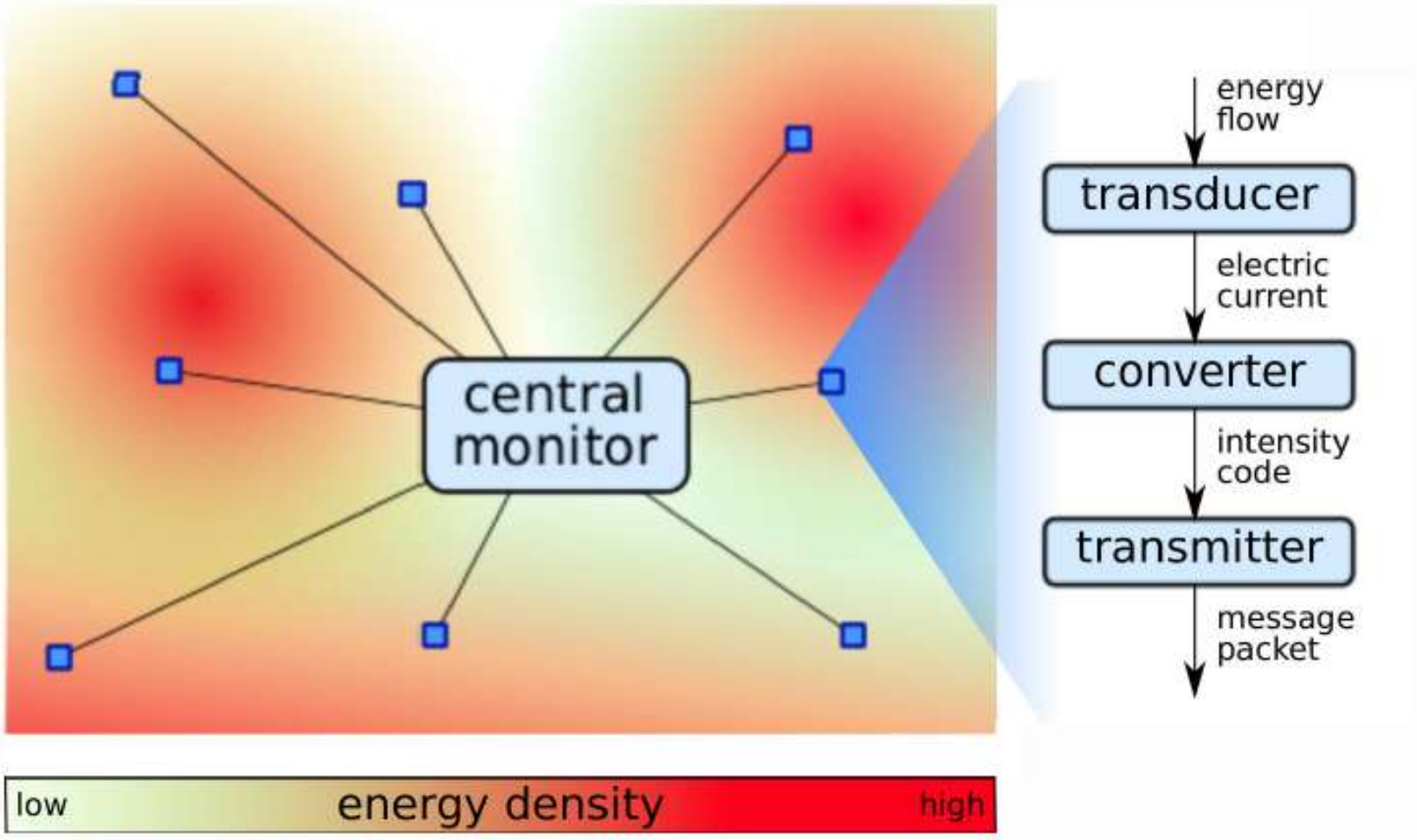
Example: condition monitoring

- Network of sensors for spaced and temporal energy mapping

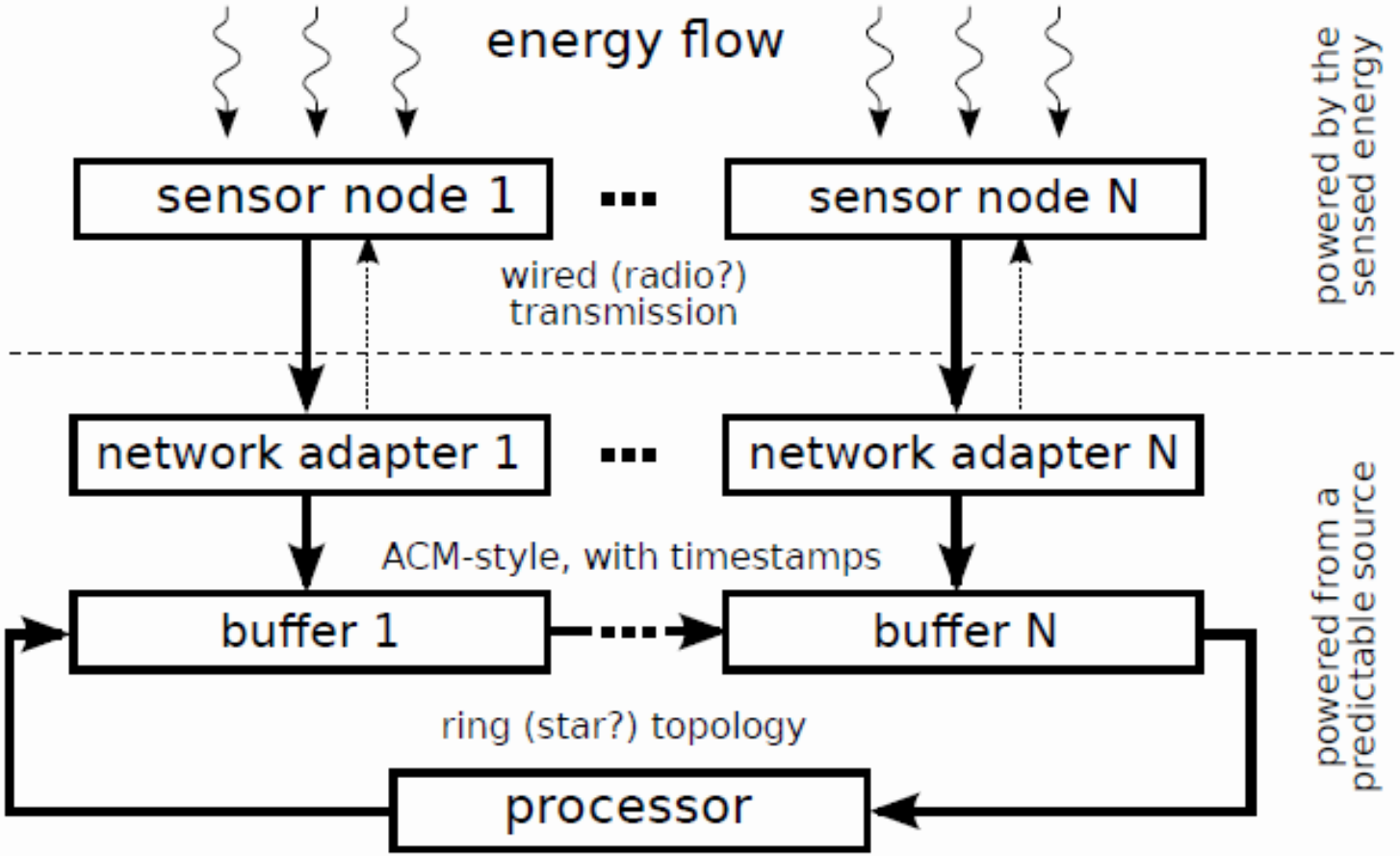


Example: condition monitoring

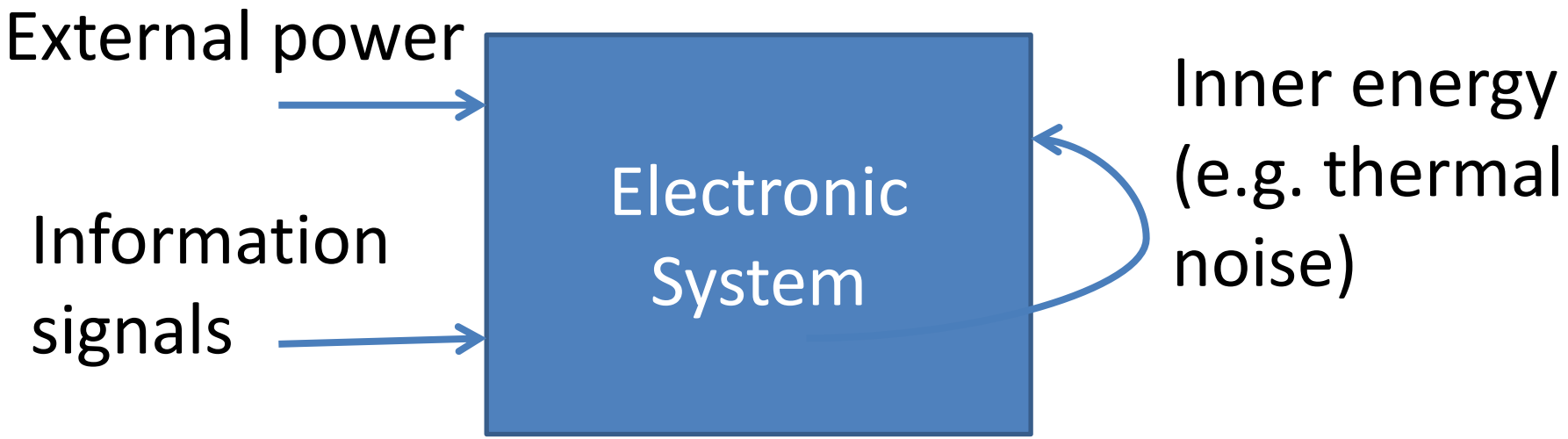
- Sensor node structure



- System architecture



Energy Theme in our Research Layers



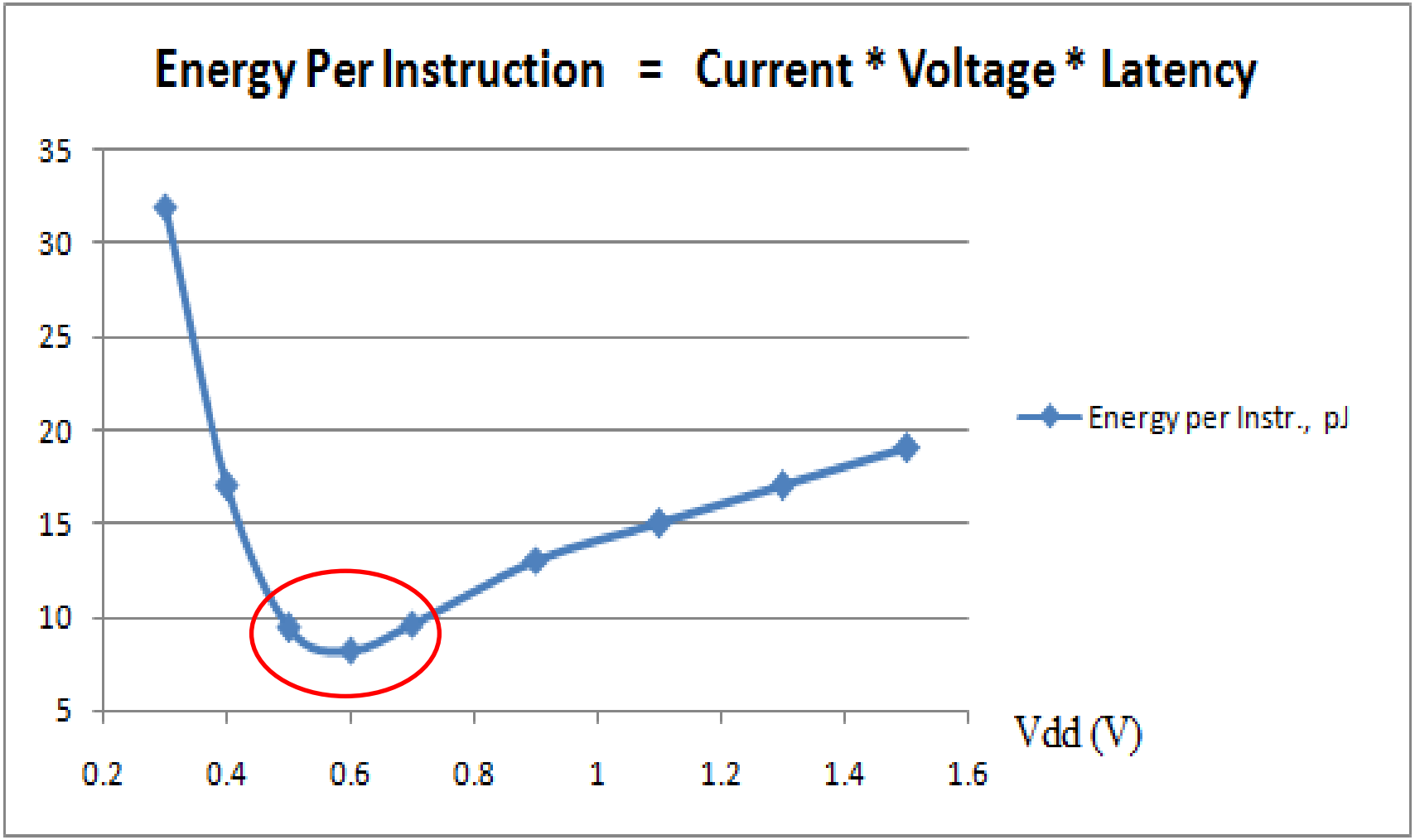
Energy in our Basic Research

- Energy & Information Processing:
  - Models of Energy and Entropy
  - Concepts of efficiency (e.g. “energy per compute”)
  - Nature is a massive computer in which energy is captured in different **form**s and quantities and constantly being trans**form**ed
  - In**form**ation processing (Computing and Comms) increasingly gleans and learns from observations in Nature as it moves closer to Nature (at least, for 4* REF papers!)

Energy in our Basic Research

- Relationship between Power and Timing
  - Power-driven timing (Freq ~ Vdd)
- Computing is largely decision making (e.g., is the value of input 0111 or 1000?)
  - Decision-making is about choice; it takes time and energy
- Energy & Information are Resources
  - Resource representation (e.g. token-based computing)
  - Modelling methods: graphs, flows, concurrency, partial orders

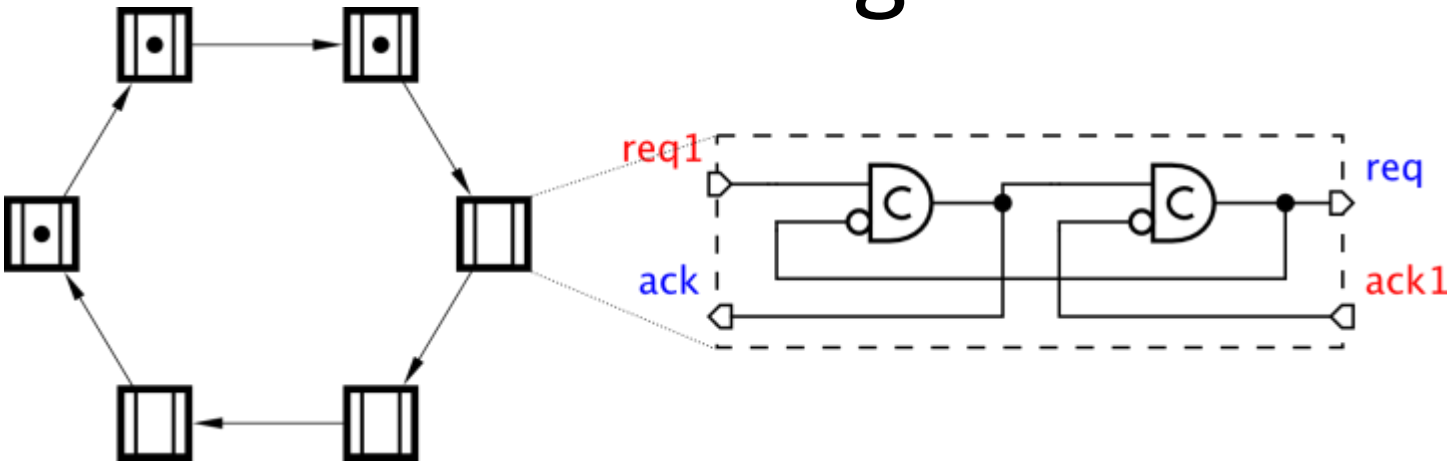
Energy Efficiency (measurements on real silicon - asynchronous 8051)



“Grand-prix” race with a fuel limit

The goal: Given a finite amount of fuel, maximize the total number of laps made all the cars on the circuit.
Unknown parameters: What is the optimum engine power? What is the optimum number of cars on the circuit?

Ring-pipeline with a finite energy budget



***Experiment*:**

a. A ring micropipeline with 5 stages is used in the experiment.

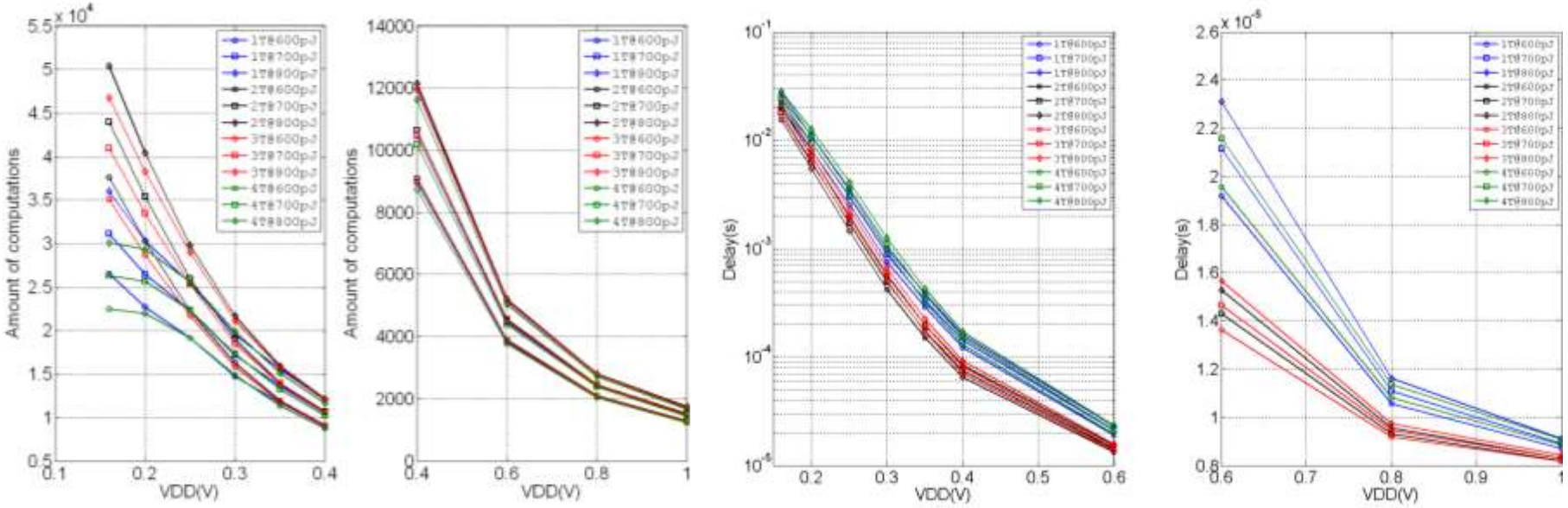
b. Simulation Results are obtained with different parallelism (1, 2, 3, 4 tokens), in different working voltages (1.0V, 0.8V, 0.6V, 0.4V, 0.35V, 0.25V, 0.2V, 0.16V), and under different amount of energy (600pJ, 700pJ, 800pJ).

c. A run stops when the energy is fully consumed.

d. The amount of computation is counted for each run.

e. A unit of computation is defined as one pulse generated in the pipeline.

Ring pipeline with a given energy budget



***Conclusions*:**

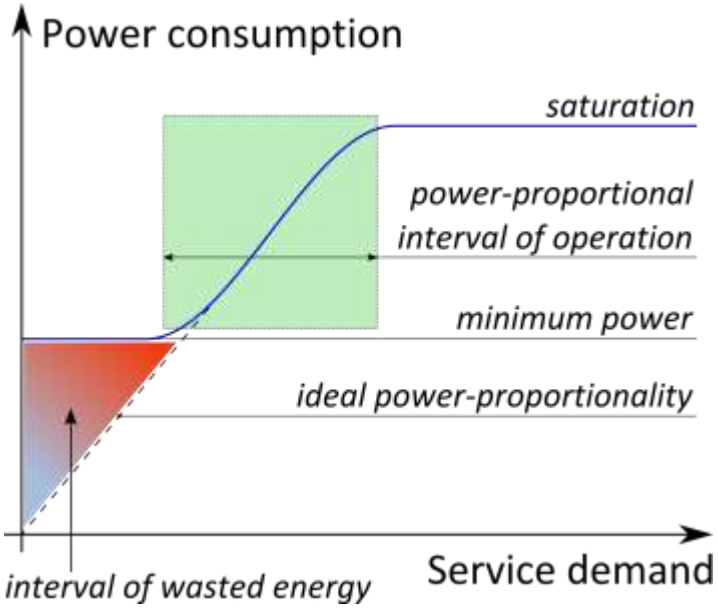
- The higher the concurrency the greater the amount of computation and the smaller the amount of leakage.
- At sub-threshold voltages, the amount of computation is STRONGLY affected by degree of concurrency, due to the effect of leakage.
- Above threshold, the amount of computation that is practically insensitive to the degree of concurrency.

Energy in our Applied Research

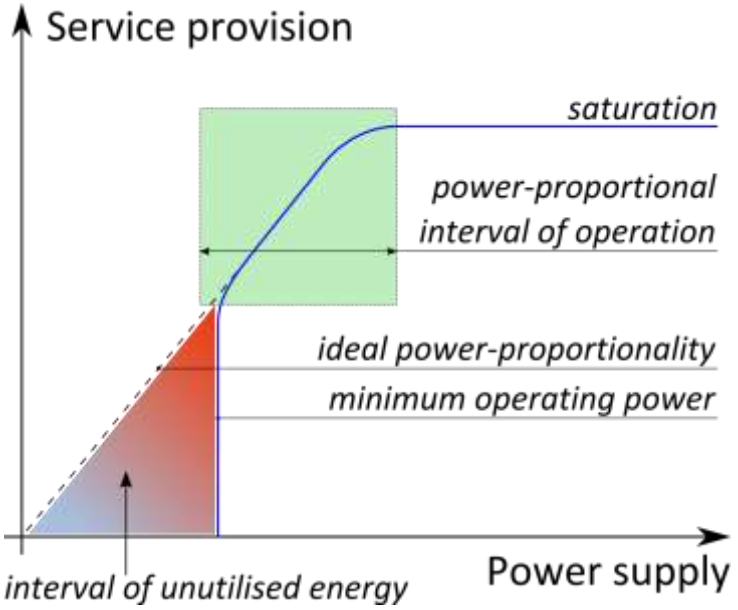
- Performance, Energy, Reliability (PER) Interplay:
  - In systems themselves (e.g. power-proportional computing) and in system design (e.g. power-proportional modelling and analysis)
- Low-Power Systems Design:
  - Event-based computing and asynchronous logic
  - “Reference-free” sensing (sensing using energy of the sensed signal)
  - Power-gating, “adiabatic” computing, near- and sub-threshold computing

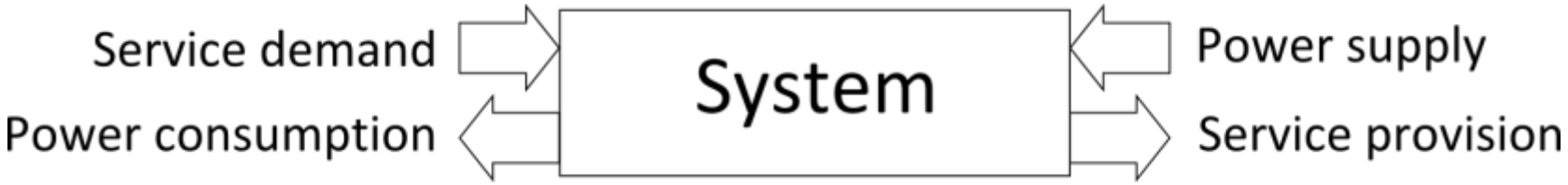
Power proportionality

Service-modulated processing

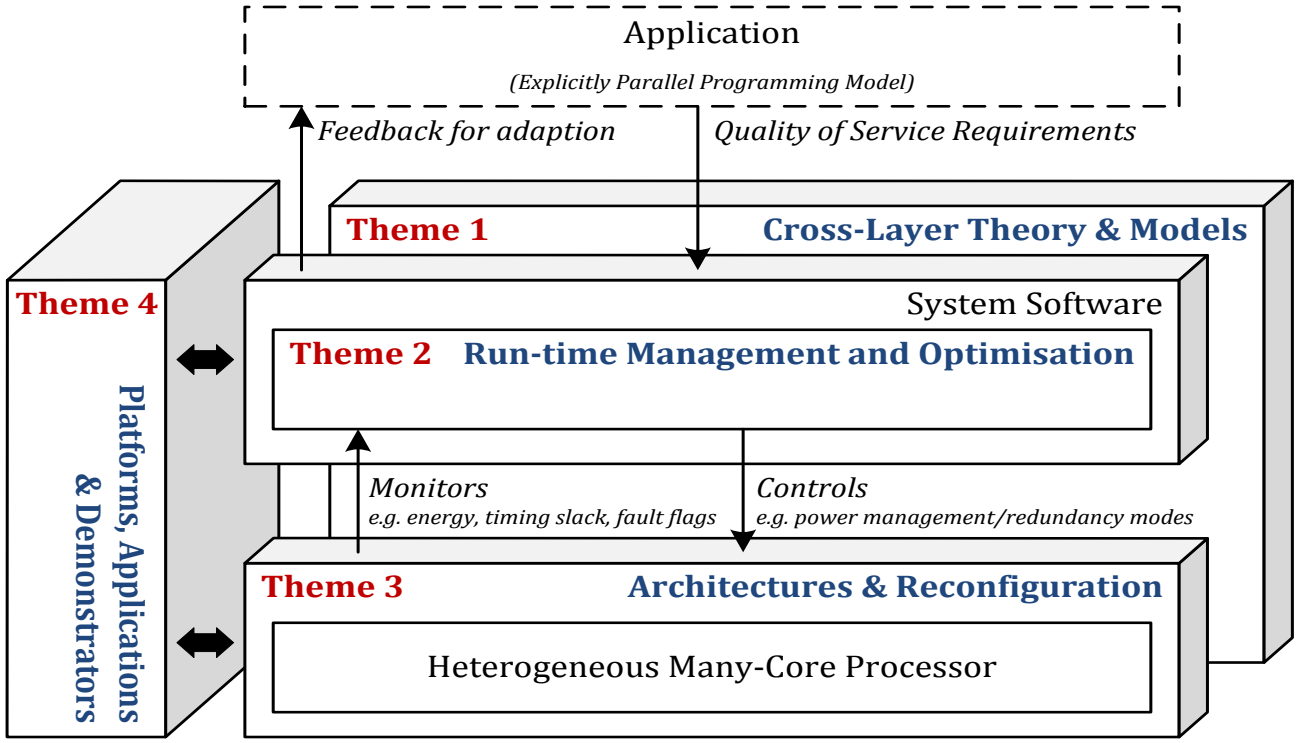


Energy-modulated processing



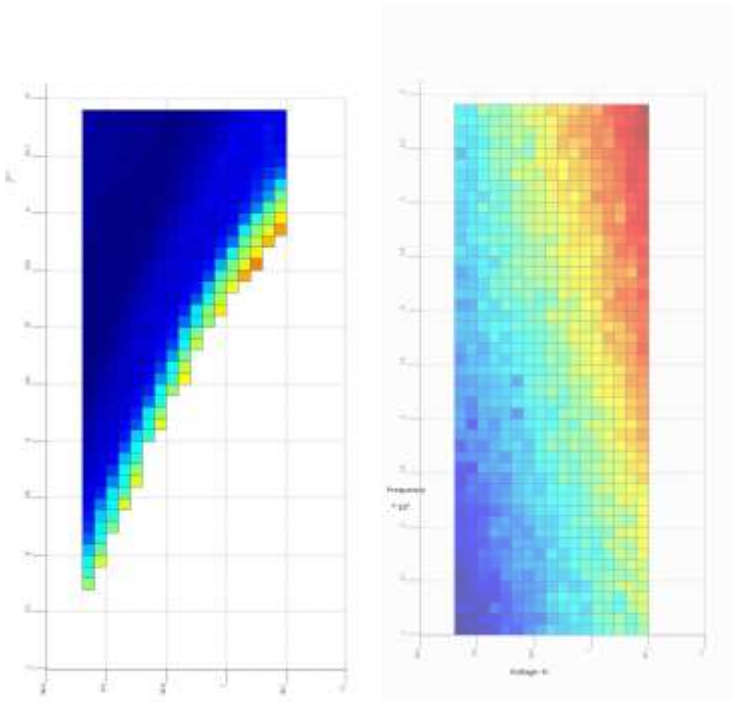


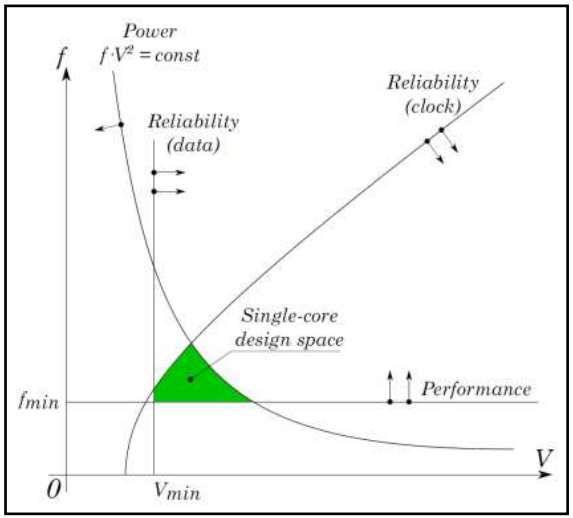
Power-efficient, **R**eliable, **M**any-core **E**mbedded systems (PRiME Project)

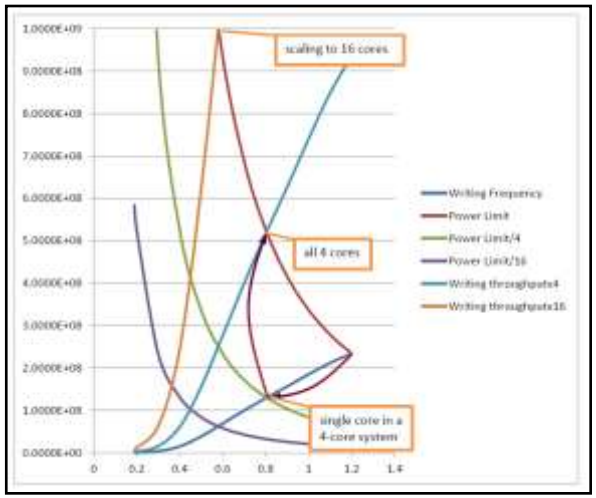


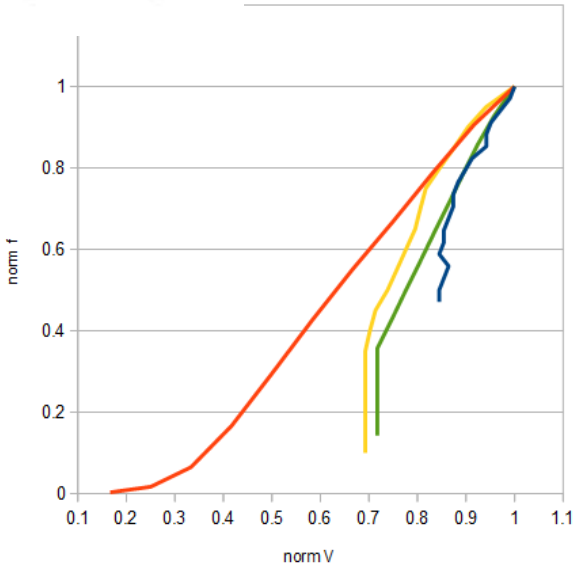
PRiME: PER modelling

- Building analytical models using actual experimental data:
  Intel's Xeon/Core, Altera FPGA, ARM-based
  Odroid and async CPU/SRAM
- Incorporating PER models into high level scalable models
- The models are used in Run-Time management of many-core systems





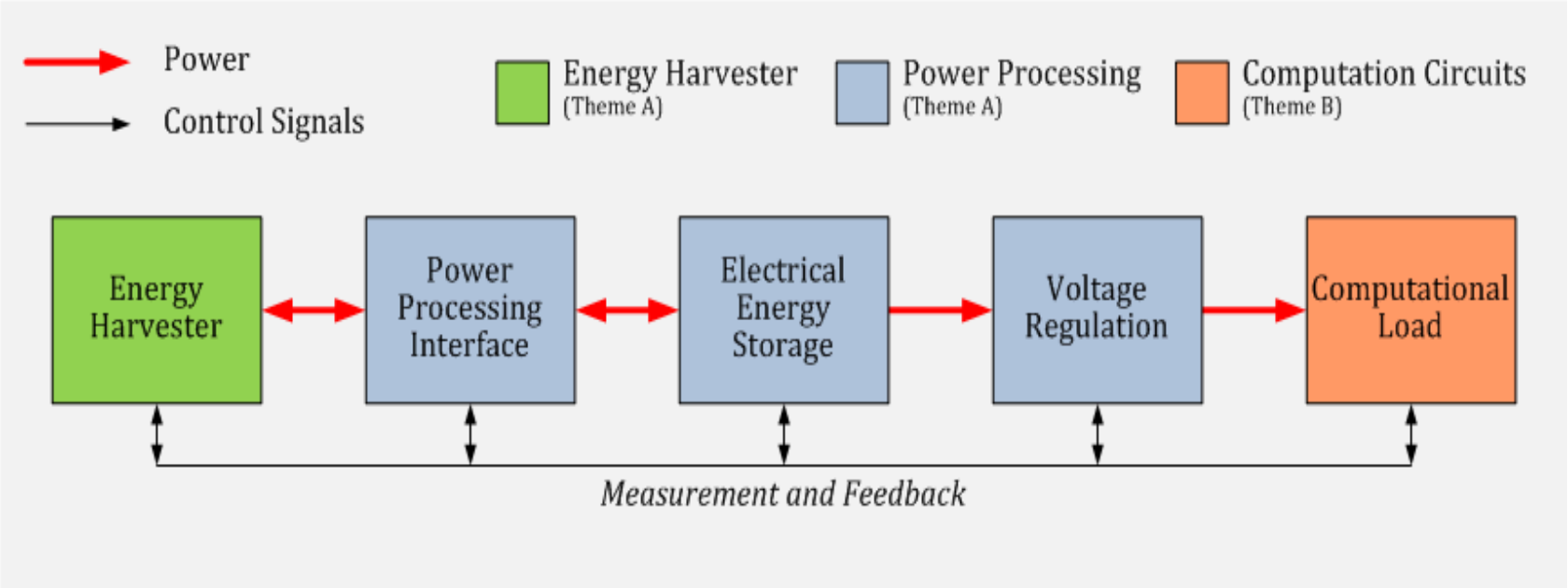




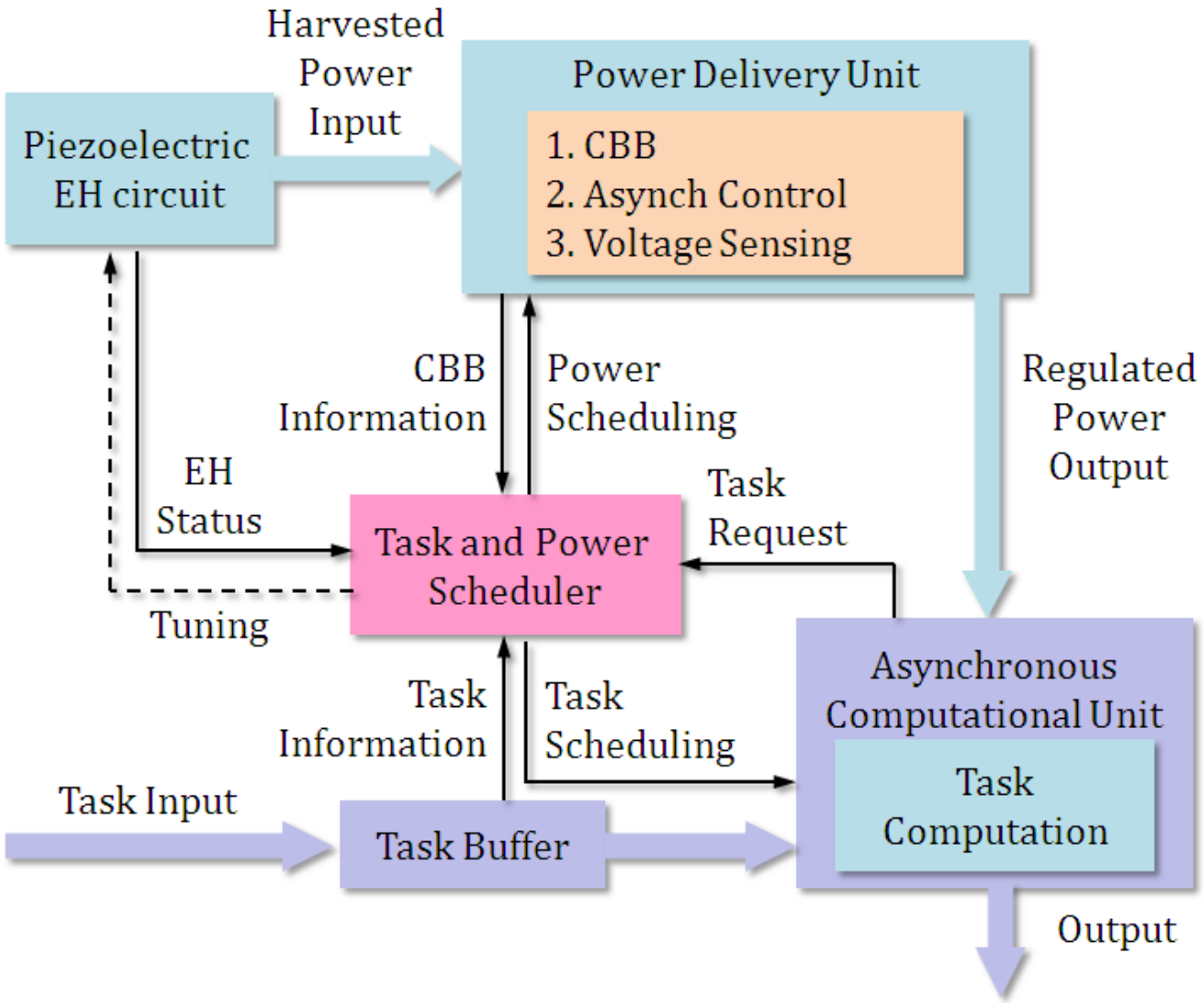
Energy in our Applied Research

- System design for autonomy and survival under variable and intermittent power:
  - Electronics for energy-harvesting
  - Mixed-criticality systems
  - Multi-layered system architectures (cf. neural systems in biology)

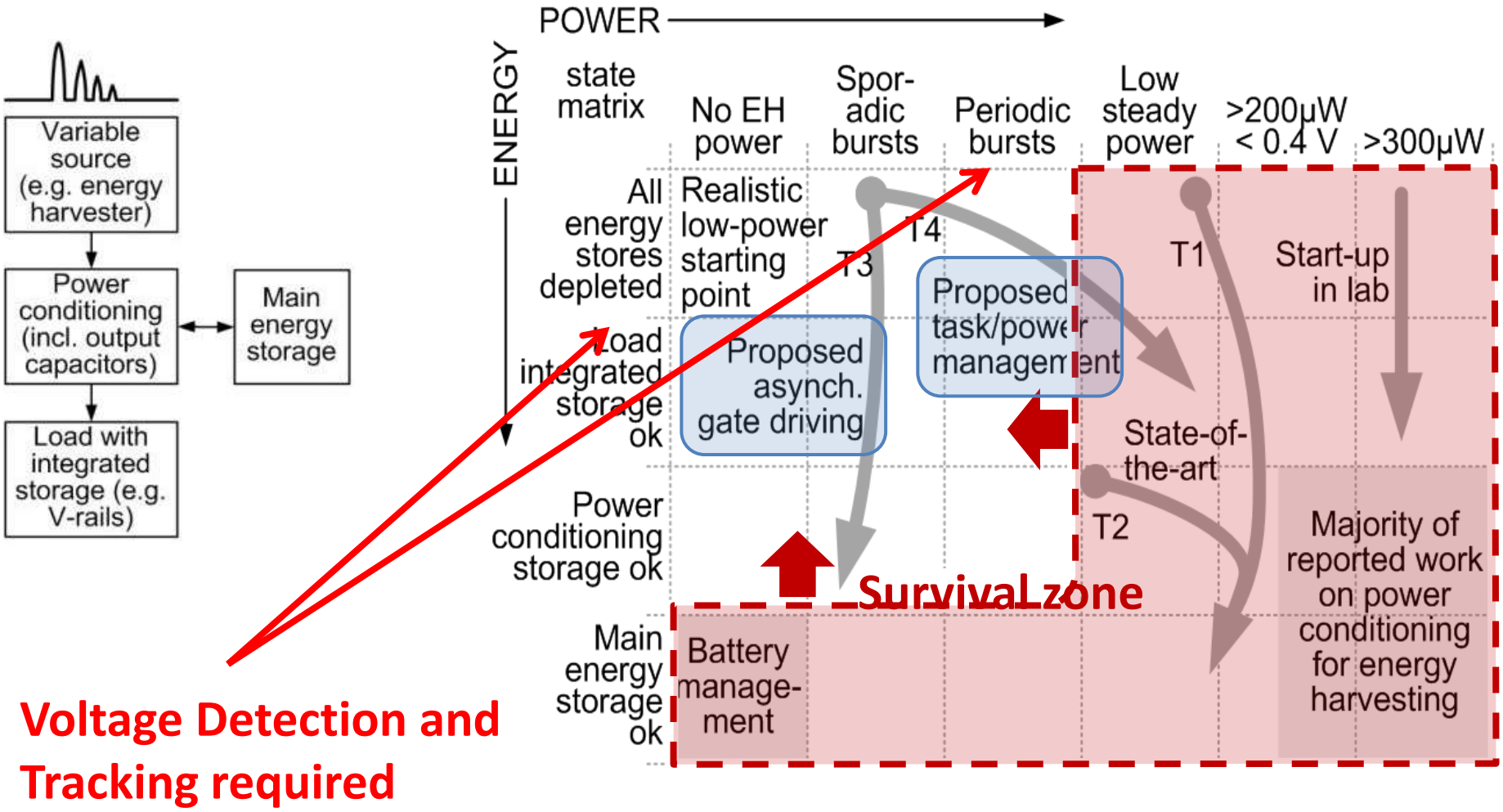
Holistic approach to EH electronics



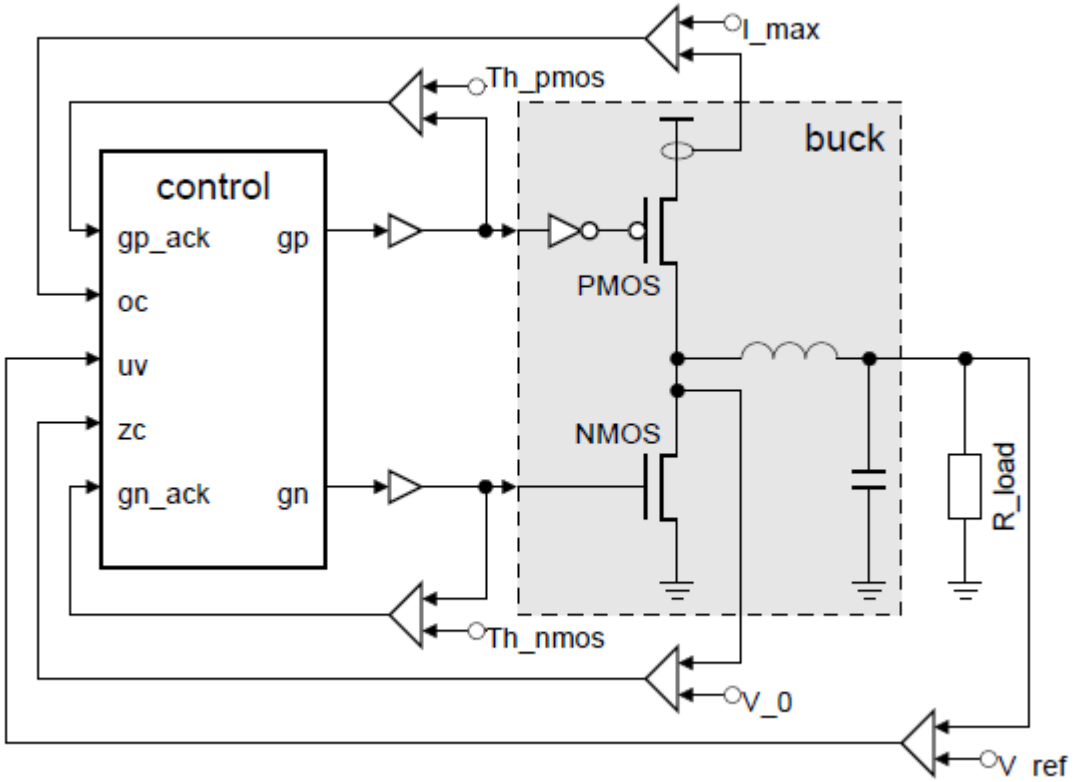
Our View on EH Systems



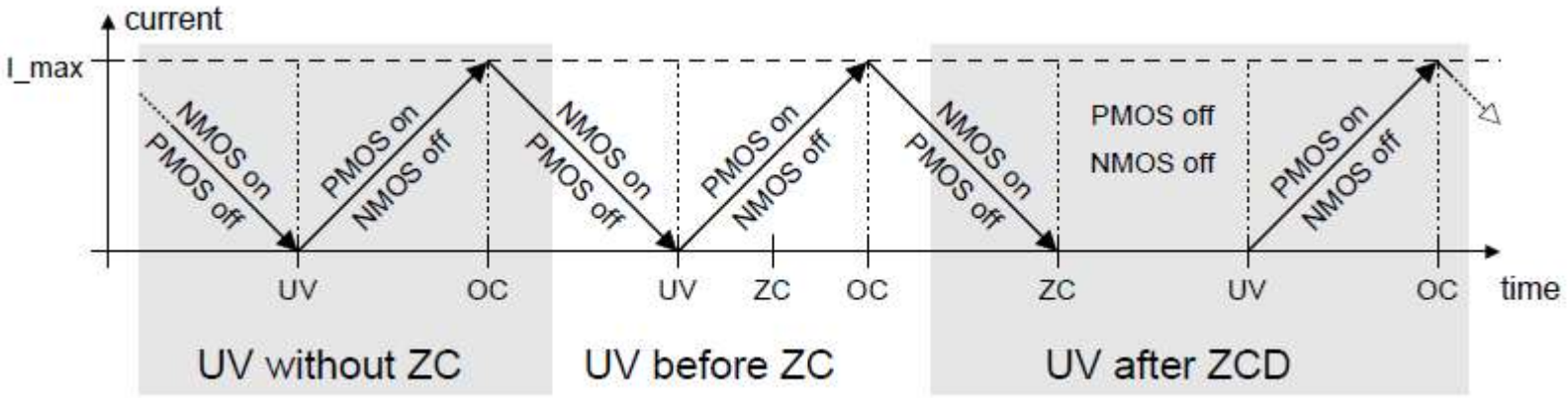
Staying alive in variable, intermittent, low-power environments (Savvie Project)

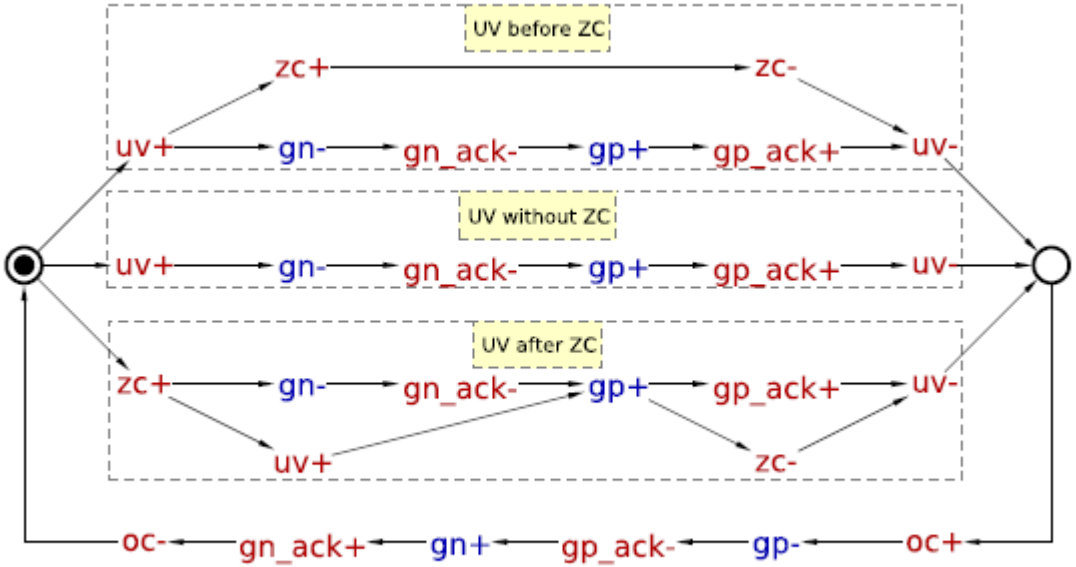


Asynchronous Design for Analogue Electronics (A4A Project)



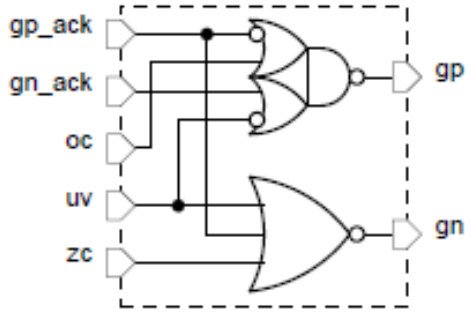
Asynchronous control for Bucks



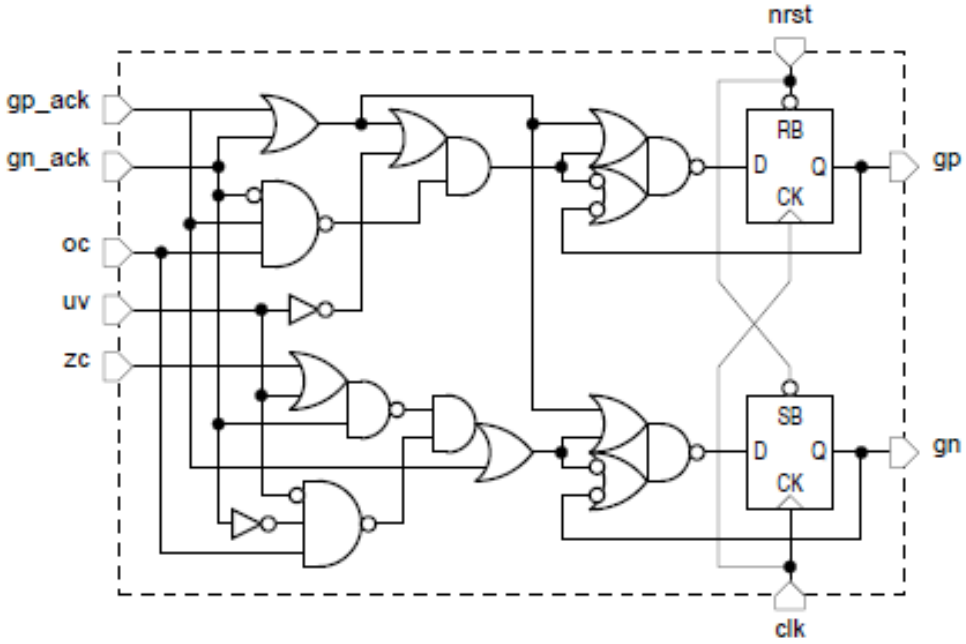


(b) Complete specification

Asynchronous control for Bucks



(a) Complex gate asynchronous implementation



(b) Synchronous implementation

Key Collaborations

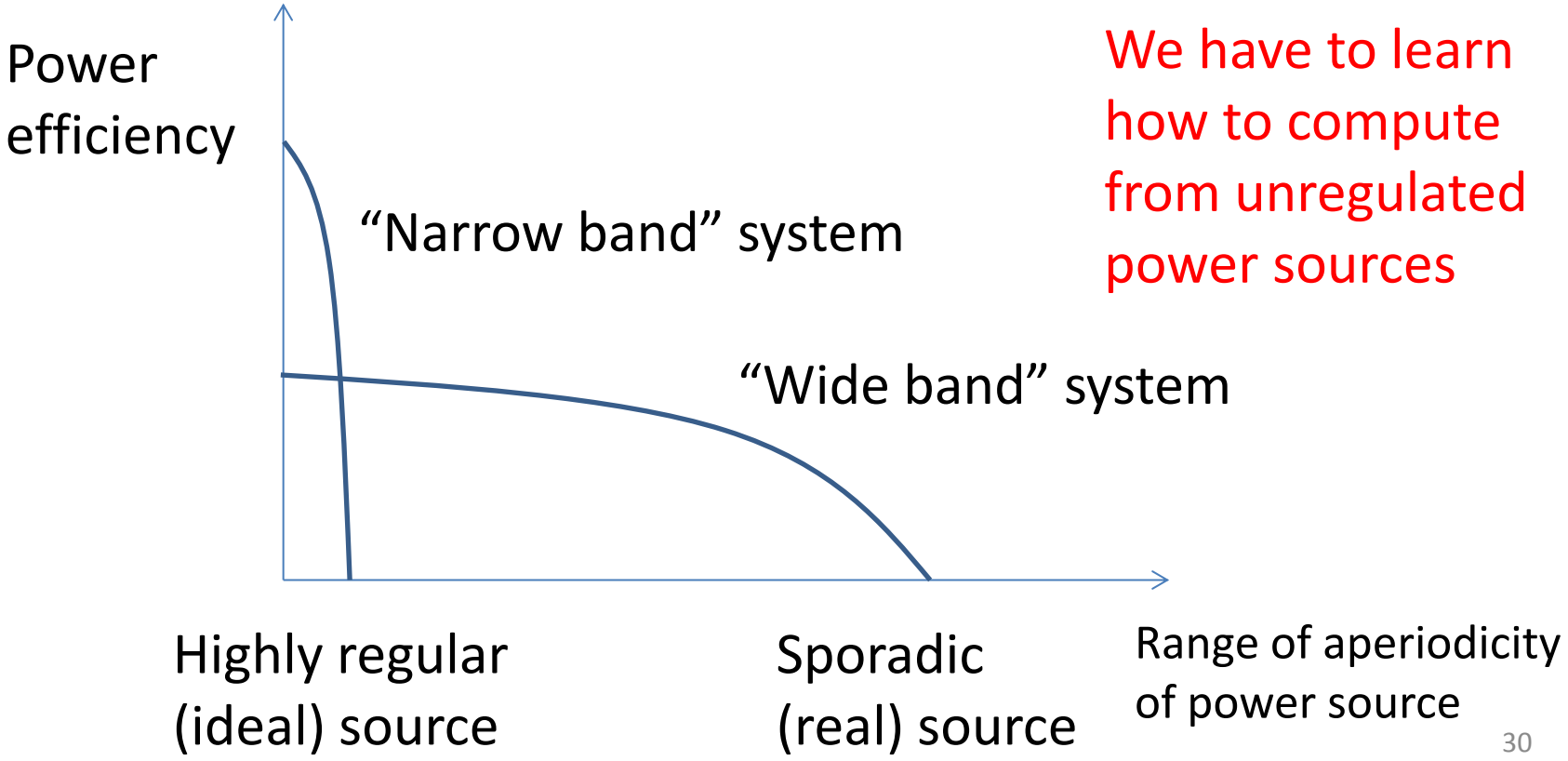
- Energy harvesting: Bristol, Imperial and Southampton
- Low power and asynchronous systems: Manchester, IHP (Germany), CEA-LETI (France), UPC (Spain), USC (USA)
- Models and Tools: Newcastle CS
- Industrial: ARM (iCASE studentship in electronics design for IoT), Dialog Semiconductor (Async design tools for power management electronics),

Key Challenges

- Theory and design tools for wide-band powered electronic systems
- Introducing non-volatility (seamless state-retention) into electronics systems for on-chip power management and survival
- Working at near-noise levels (e.g. for CMOS: <=50mV); scavenging from inner and external noise
- Design automation for mixed-signal electronics (avoiding many hours of simulations)

Power efficiency and regularity

- Modern systems rely on highly regular (periodic) power sources – they "invest" some power into power regulation
- Future systems will have to operate in a wide dynamic range, paying the price in efficiency in a particular band



Vision for Future

Power-modulated multi-layer system

- Multiple layers of the system design can turn on at different power levels (analogies with living organisms' nervous systems or underwater life, layers of different cost labour in resilient economies)
- As power goes higher new layers turn on, while the lower layers ("back up") remain active
- The more active layers the system has the more power resourceful it is